

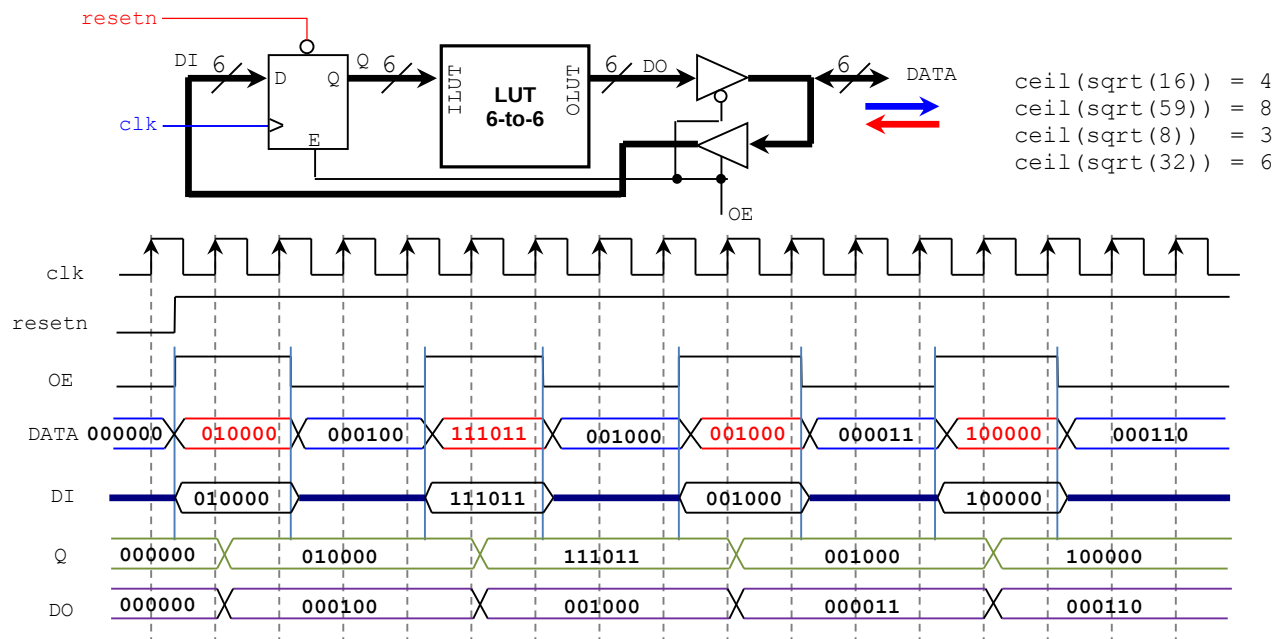
Solutions - Final Exam

(December 8th @ 7:00 pm)

Presentation and clarity are very important! Show your procedure!

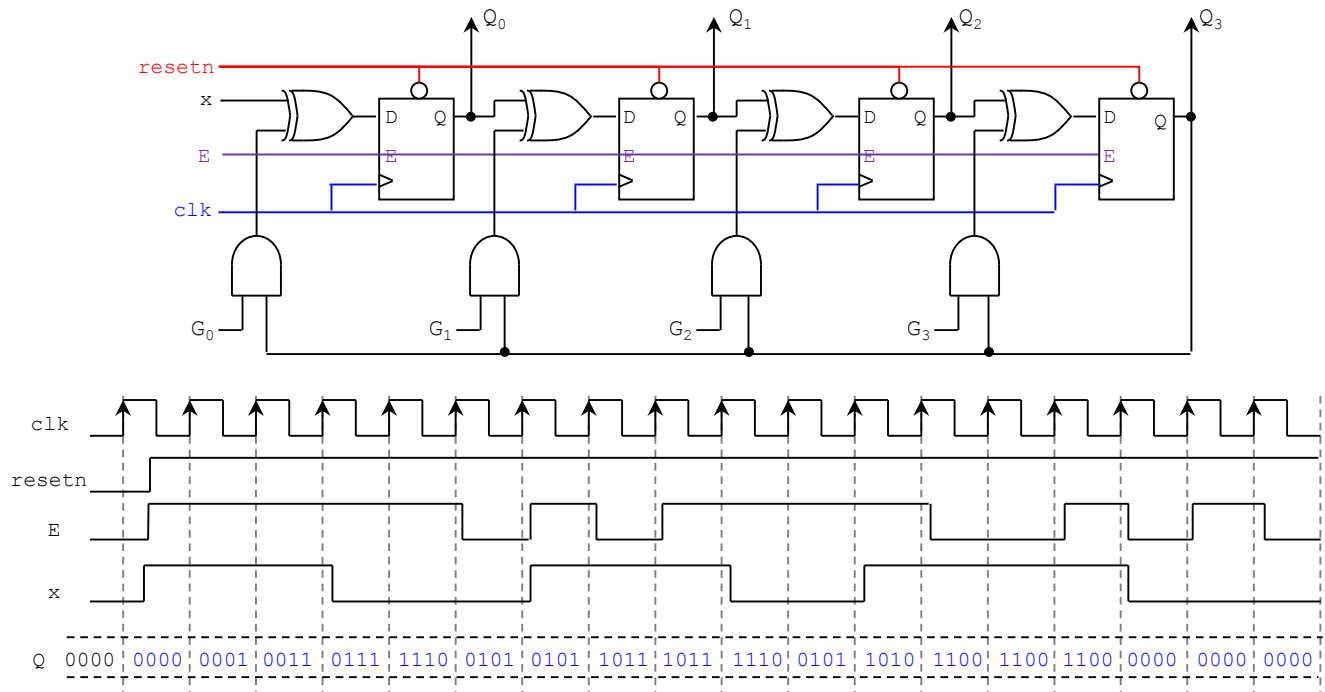
PROBLEM 1 (12 PTS)

- Given the following circuit, complete the timing diagram.
The LUT 6-to-6 implements the following function: $OLUT = \lceil \sqrt{ILUT} \rceil$, where $ILUT$ is a 6-bit unsigned number.
For example $ILUT = 35 (10011_2) \rightarrow OLUT = \lceil \sqrt{35} \rceil = 6 (000110_2)$



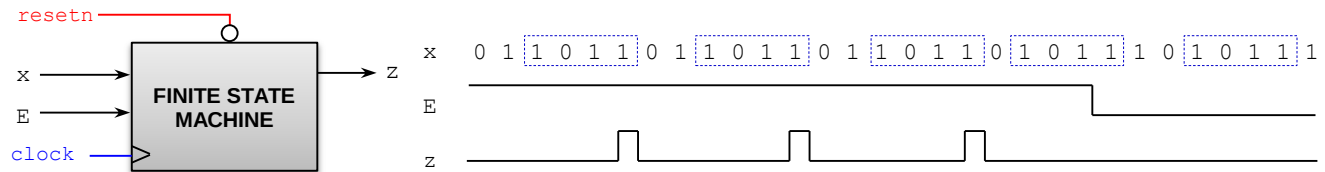
PROBLEM 2 (12 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1001$, $Q = Q_3Q_2Q_1Q_0$



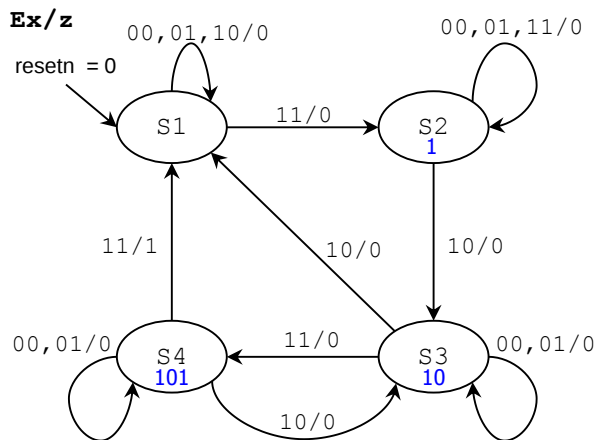
PROBLEM 3 (22 PTS)

- Sequence detector: The machine has to generate $z = 1$ when it detects the sequence 1011. Once the sequence is detected, the circuit looks for a new sequence.
- The signal E is an input enable: It validates the input x , i.e., if $E = 1$, x is valid, otherwise x is not valid.



- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit with inputs E and x and output z . Is this a Mealy or a Moore machine? Why? (15 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (4 pts)
- Sketch the circuit. (3 pts)

State Diagram, State Table, and Excitation Table:



State Assignment:

S1: $Q_1Q_0 = 00$ S2: $Q_1Q_0 = 01$
S3: $Q_1Q_0 = 10$ S4: $Q_1Q_0 = 11$

		PRESENT STATE		NEXT STATE	z	PRESENT STATE		NEXT STATE		z
E	x	STATE	STATE	STATE		E	x	$Q_1Q_0(t)$	$Q_1Q_0(t+1)$	
0	0	S1	S1	S1	0	0	0	00	00	0
0	0	S2	S2	S2	0	0	0	01	01	0
0	0	S3	S3	S3	0	0	0	10	10	0
0	0	S4	S4	S4	0	0	0	11	11	0
0	1	S1	S1	S1	0	0	1	00	00	0
0	1	S2	S2	S2	0	0	1	01	01	0
0	1	S3	S3	S3	0	0	1	10	10	0
0	1	S4	S4	S4	0	0	1	11	11	0
1	0	S1	S1	S1	0	1	0	00	00	0
1	0	S2	S3	S3	0	1	0	01	10	0
1	0	S3	S1	S1	0	1	0	10	00	0
1	0	S4	S3	S3	0	1	0	11	10	0
1	1	S1	S2	S2	0	1	1	00	01	0
1	1	S2	S2	S2	0	1	1	01	01	0
1	1	S3	S4	S4	0	1	1	10	11	0
1	1	S4	S1	S1	1	1	1	11	00	1

This is a Mealy Machine. The output 'z' depends on the input as well as on the present state.

- Excitation equations, minimization, and circuit implementation:

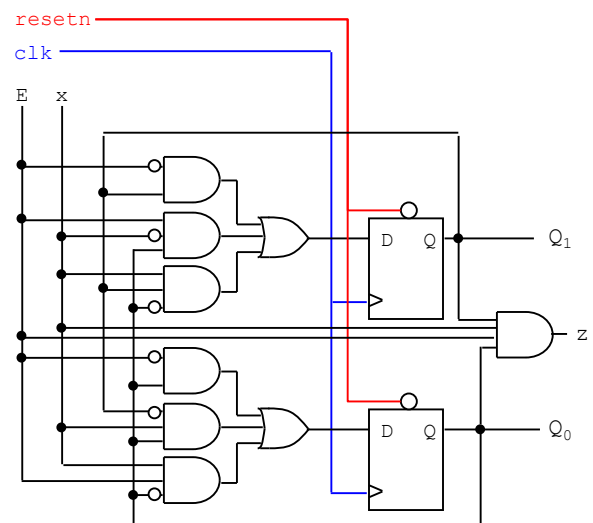
$$Q_1(t+1) = \bar{E}Q_1 + E\bar{x}Q_0 + xQ_1\bar{Q}_0$$

$$Q_0(t+1) = \bar{E}Q_0 + Ex\bar{Q}_0 + x\bar{Q}_1Q_0$$

$$z = ExQ_1Q_0$$

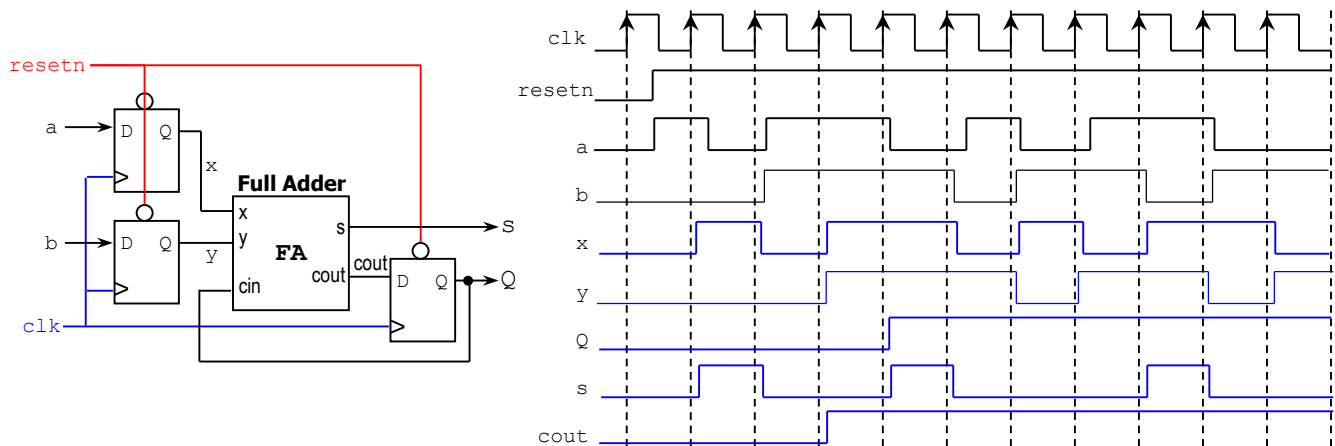
Ex	00	01	11	10
00	0	0	0	0
01	0	0	0	1
11	1	1	0	1
10	1	1	1	0

Ex	00	01	11	10
00	0	0	1	0
01	1	1	1	0
11	1	1	0	0
10	0	0	1	0



PROBLEM 4 (20 PTS)

- Complete the timing diagram of the circuit shown below: (8 pts)



- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following Finite State Machine: (12 pts)

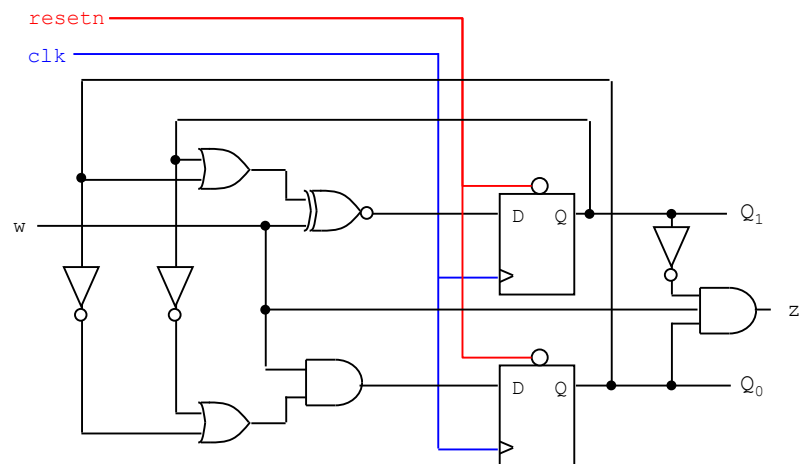
$$Q_1(t+1) = \overline{(Q_1 + Q_0) \oplus w}$$

$$Q_0(t+1) = Q_1 Q_0 w$$

$$z = w Q_1 Q_0$$

State Assignment:

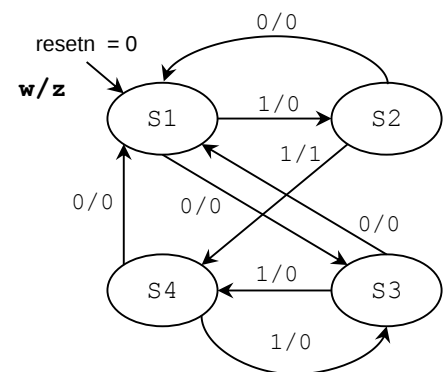
S1: Q=00 S2: Q=01
S3: Q=10 S4: Q=11



PRESENT STATE			NEXTSTATE	
w	Q ₁ Q ₀ (t)		Q ₁ Q ₀ (t+1)	z
0	0 0		1 0	0
0	0 1		0 0	0
0	1 0		0 0	0
0	1 1		0 0	0
1	0 0		0 1	0
1	0 1		1 1	1
1	1 0		1 1	0
1	1 1		1 0	0



PRESENT STATE		NEXT STATE	
w	STATE	STATE	z
0	S1	S3	0
0	S2	S1	0
0	S3	S1	0
0	S4	S1	0
1	S1	S2	0
1	S2	S4	1
1	S3	S4	0
1	S4	S3	0

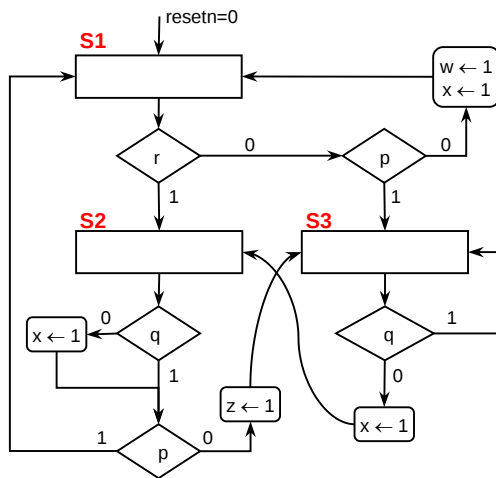


PROBLEM 5 (16 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description is shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

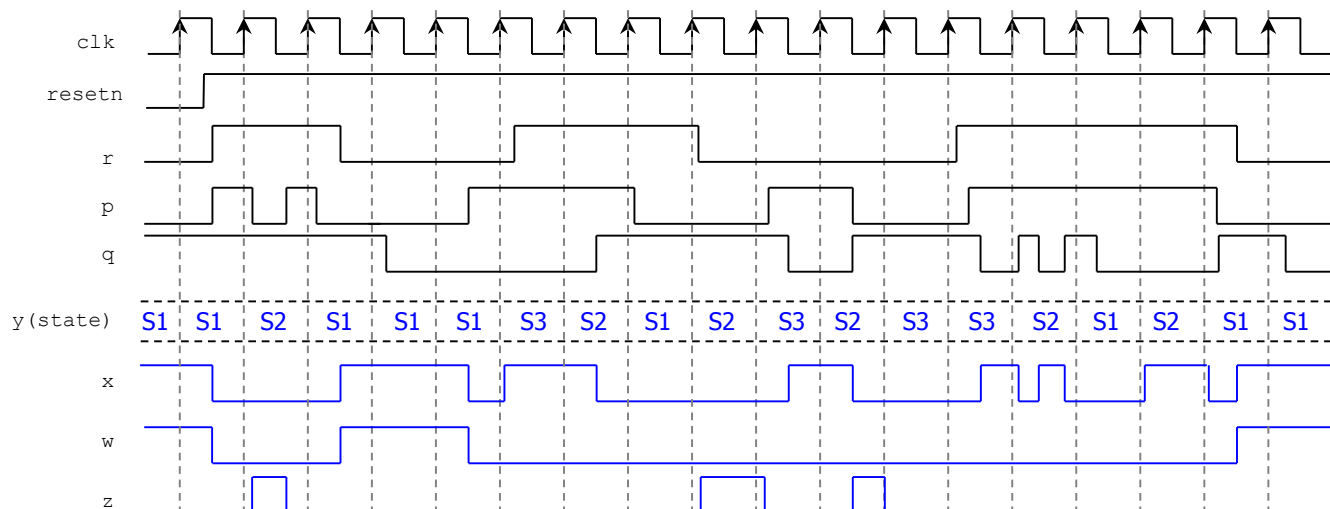
entity circ is
    port ( clk, resetn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;
```



```
architecture behavioral of circ is
    type state is (S1, S2, S3);
    signal y: state;
begin
    Transitions: process (resetn, clk, r, p, q)
    begin
        if resetn = '0' then y <= S1;
        elsif (clk'event and clk = '1') then
            case y is
                when S1 =>
                    if r = '1' then
                        y <= S2;
                    else
                        if p = '1' then y <= S3; else y <= S1; end if;
                    end if;
                when S2 =>
                    if p = '1' then y <= S1; else y <= S3; end if;
                when S3 =>
                    if q = '1' then y <= S3; else y <= S2; end if;
            end case;
        end if;
    end process;

    Outputs: process (y, r, p, q)
    begin
        x <= '0'; w <= '0'; z <= '0';
        case y is
            when S1 => if r = '0' then
                            if p = '0' then
                                w <= '1'; x <= '1';
                            end if;
                        end if;
            when S2 => if q = '0' then x <= '1'; end if;
                            if p = '0' then z <= '1'; end if;
            when S3 => if q = '0' then x <= '1'; end if;
        end case;
    end process;
end behavioral;
```

This is a Mealy Machine. The outputs 'x,w,z' depend on the input as well as on the present state.



PROBLEM 6 (18 PTS)

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.

